



EMIF03-SIM01

IPAD™

3 LINES EMI FILTER AND ESD PROTECTION

MAIN PRODUCT APPLICATIONS

EMI filtering and ESD protection for :

- SIM Interface (Subscriber Identify Module)
- UIM Interface (Universal Identify Module)

DESCRIPTION

The EMIF03-SIM01 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF03 Flip Chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

BENEFITS

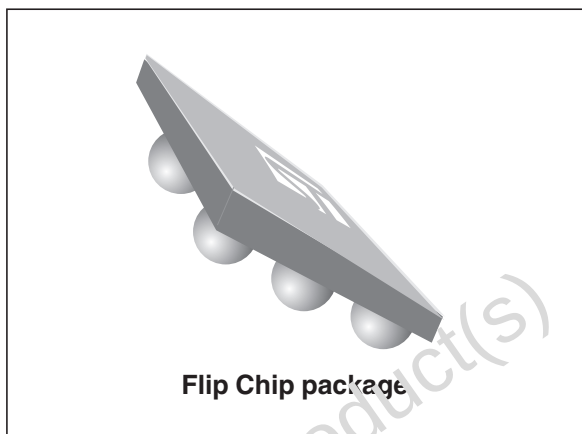
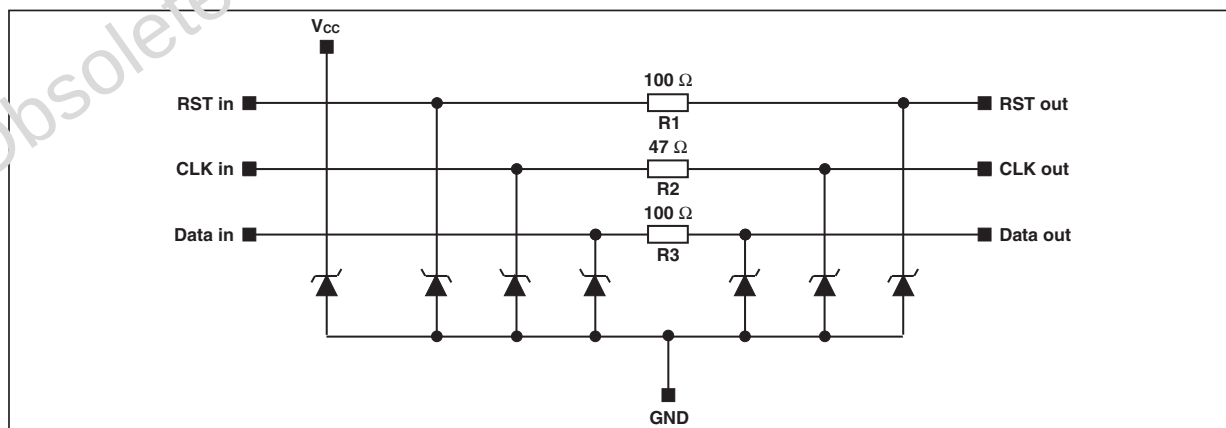
- EMI symmetrical (I/O) low-pass-filter
- High efficiency in EMI filtering
- Very low PCB space consuming:
1.57mm x 1.57 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS :

IEC61000-4-2 15kV (air discharge)
8 kV (contact discharge)

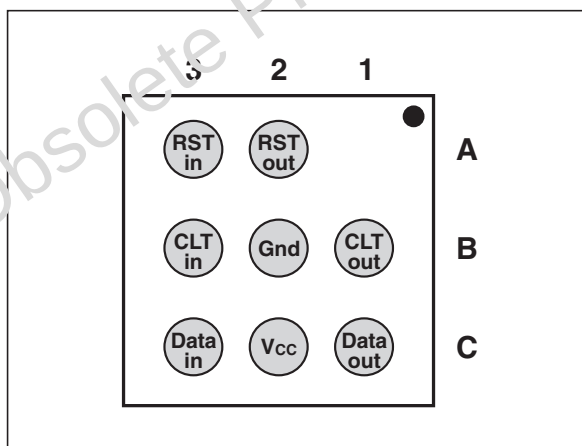
MIL STD 883E - Method 3015-6 Class 3

CONFIGURATION



Flip Chip package

PIN CONFIGURATION (Ball side)



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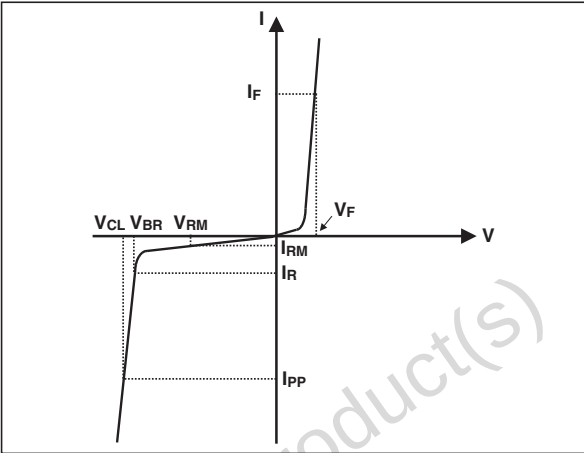
July 2003 - Ed: 8A

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T _j	Maximum junction temperature	125	°C
T _{op}	Operating temperature range	-40 to + 85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter
V _{BR}	Breakdown voltage
I _{RM}	Leakage current @ V _{RM}
V _{RM}	Stand-off voltage
V _{CL}	Clamping voltage
R _d	Dynamic impedance
I _{PP}	Peak pulse current
R _{I/O}	Series resistance between Input & Output
C _{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V _{BR}	I _R = 1 mA	6			V
I _{RM}	V _{RM} = 3V			1	μA
R _d			1.5		Ω
R ₁		95	100	105	Ω
R ₂		44.65	47	49.35	Ω
R ₃		95	100	105	Ω
C _{line}	@ 0V			35	pF

Fig. 1: S21 (dB) attenuation measurements.

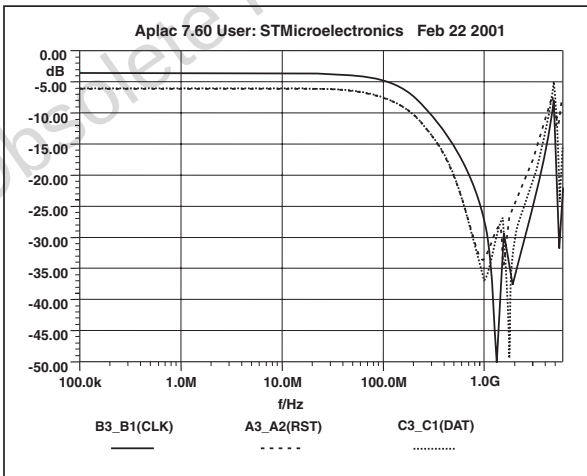


Fig. 2: Analog crosstalk measurements.

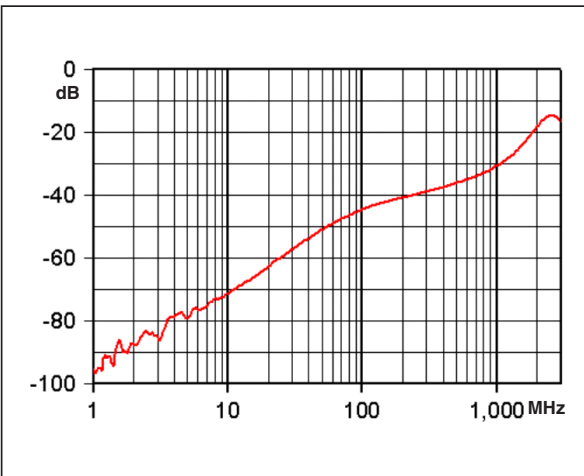
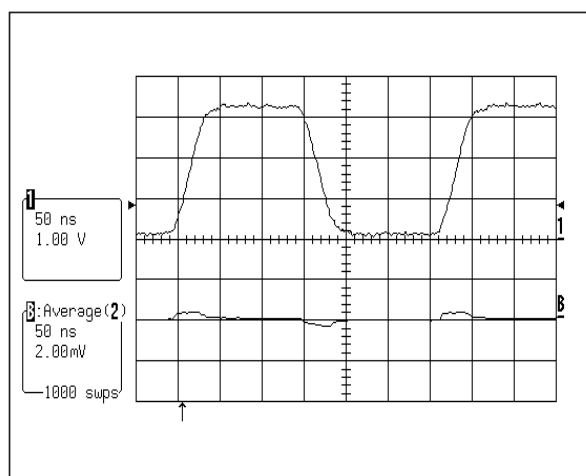
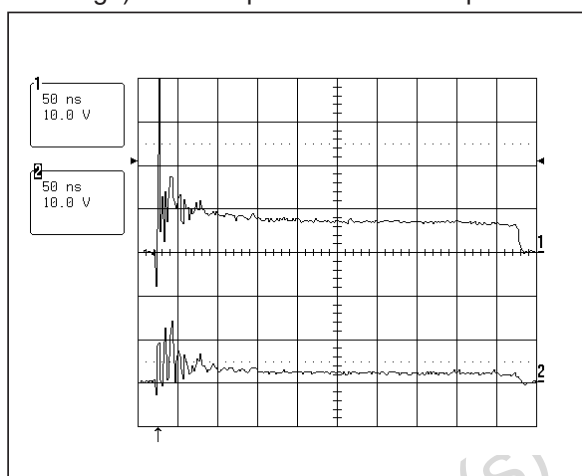
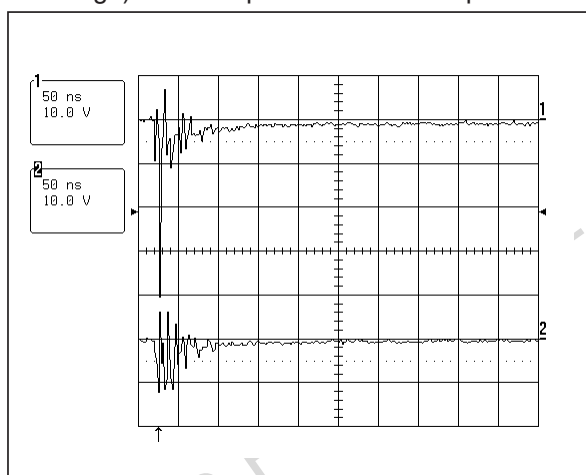
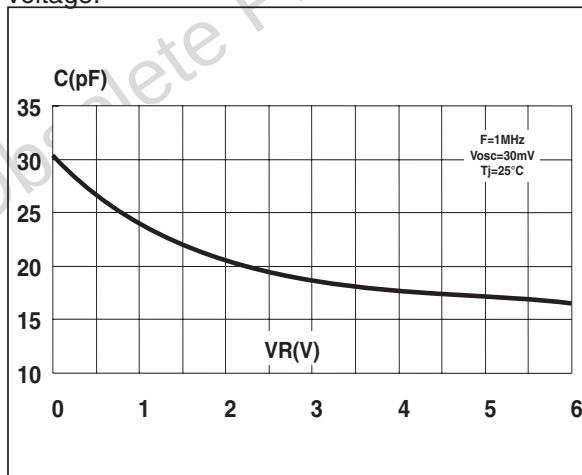
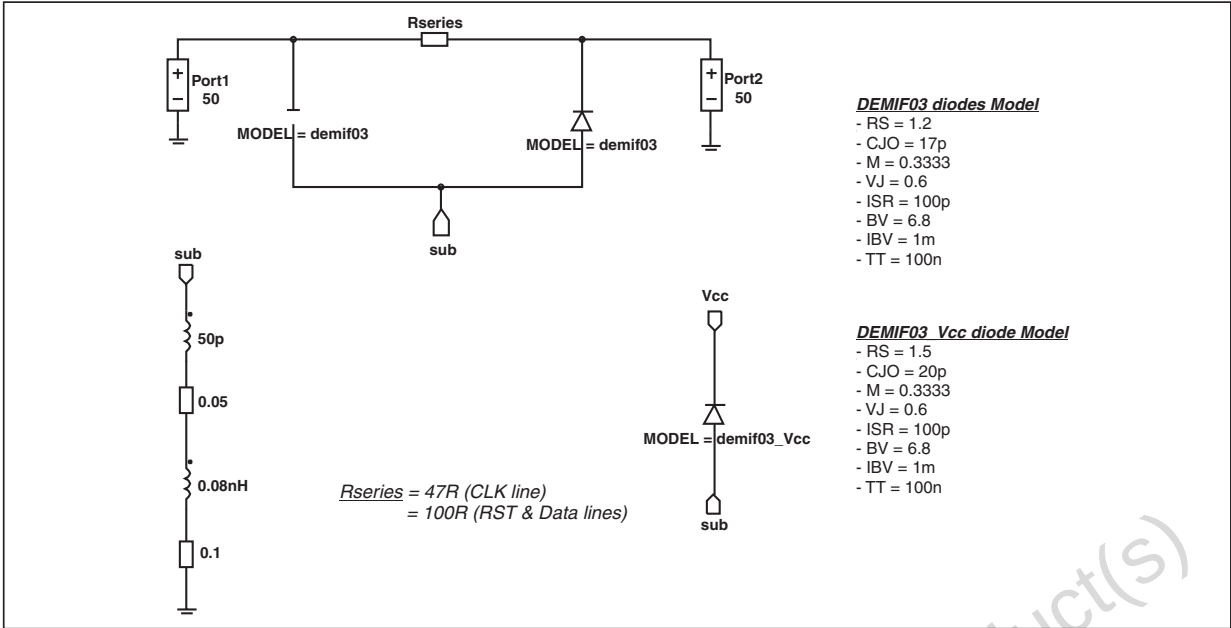


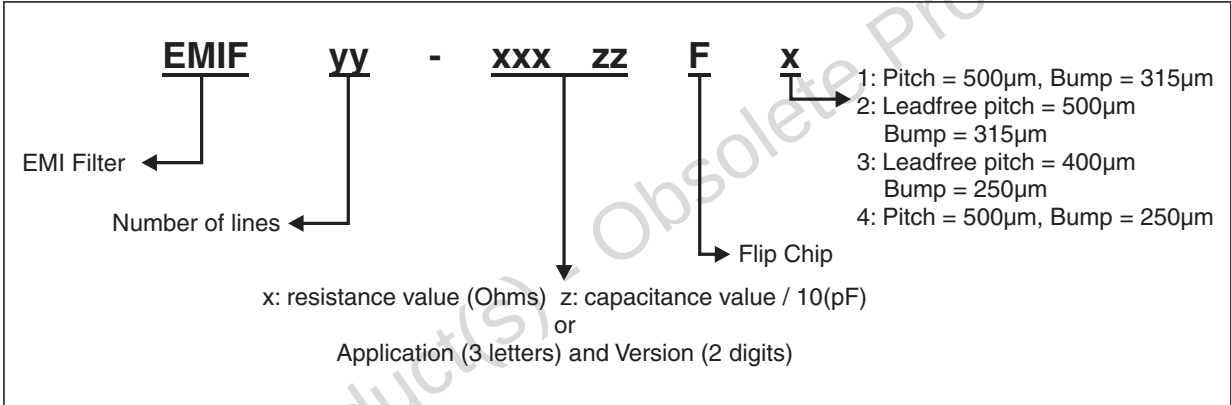
Fig. 3: Digital crosstalk measurements.**Fig. 4:** ESD response to IEC61000-4-2 (+15kV air discharge) on one input and on one output.**Fig. 5:** ESD response to IEC61000-4-2 (-15kV air discharge) on one input and on one output.**Fig. 6:** Line capacitance versus reverse applied voltage.

EMIF03-SIM01

Aplac model

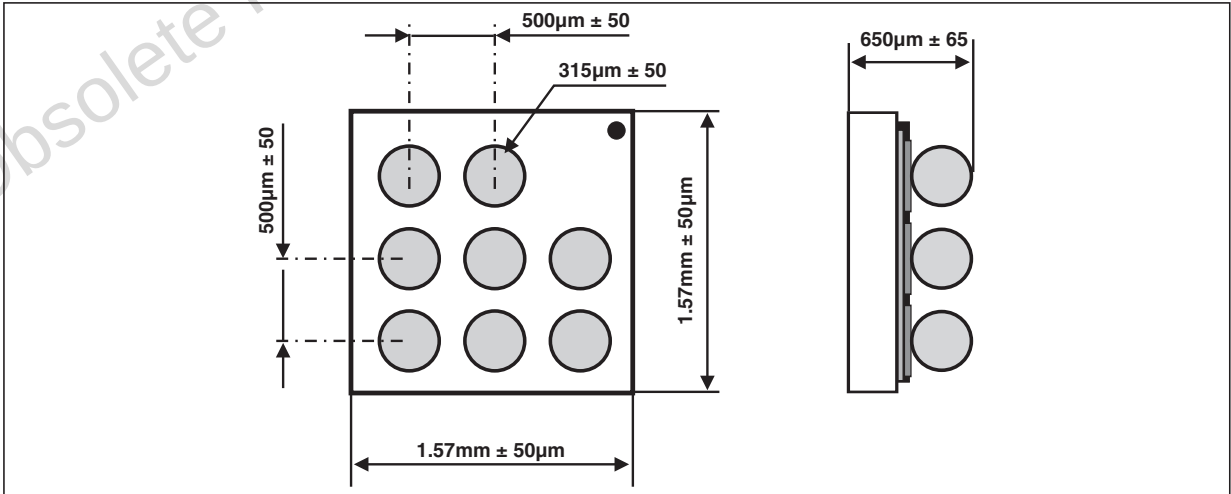


ORDER CODE

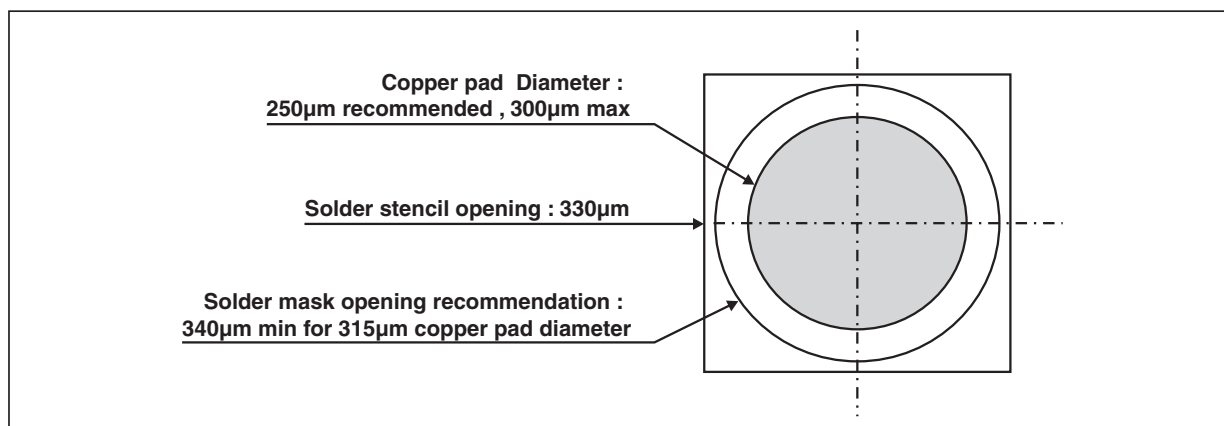


PACKAGE MECHANICAL DATA

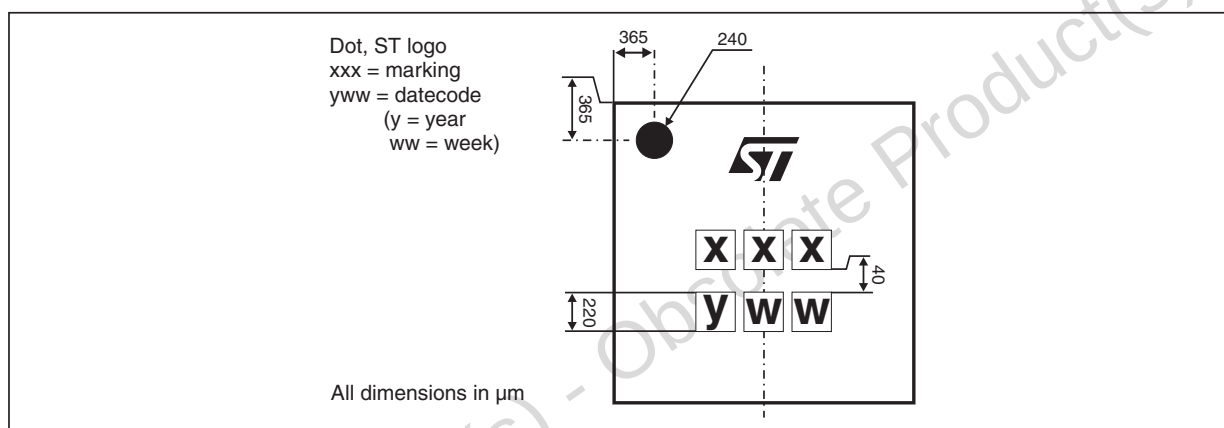
(all dimensions in μm)



FOOT PRINT RECOMMENDATIONS



MARKING





Note: More packing information are available in the application note AN1235: “Flip-Chip: Package description and recommendations for use”

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6/6